# USING SHARING TREES IN THE AUTOMATED ANALYSIS OF REAL-TIME SYSTEMS WITH DATA.

David Kendall William Henderson Adrian Robson

Department of Computing and Mathematics, University of Northumbria at Newcastle, Ellison Building, New
astle upon Tyne, NE1 8ST

Rea
hability analysis and model he
king of timed automata are now well-established te
hniques in the analysis of real-time control systems. The major limiting factor in their use, from a technical point of view, remains the state explosion problem. Symboli representation of the state spa
e often allows for the analysis of mu
h larger systems than the point-wise representation whi
h is ommon in enumerative analysis. In parti
ular, the use of rooted, ordered binary decision diagrams (ROBDDs) has been successful, mainly in the analysis of hardware systems where the need for a ompa
t representation of boolean fun
 tions is prevalent. However in software systems, it is often desirable to represent data types whi
h are more ompli
ated than booleans. The use of sharing trees [16], which eliminates the requirement to find a boolean encoding of all data types, may offer a more attra
tive alternative to ROBDDs in these circumstances. This paper considers the use of sharing trees in the ontext of automata derived from a timed algebra of asyn
hronous broad
asting systems. It suggests that an encoding of timing constraints may be more easily in
orporated into a sharing tree representation of the state spa
e than into one based on ROBDDs.

## 1 Introdu
tion

This paper outlines an approa
h to the implementation of rea
hability analysis of timed automata derived from system models des
ribed using a timed pro
ess algebra. It suggests that the sharing tree data structure provides a compact encoding of both the dis
rete and ontinuous omponents of a state vector. The rest of the paper is organised as follows: section 2 briefly introduces CANDLE [10], a language for modelling broad
asting real-time systems, which includes many of the features which one wishes to handle in automated analysis; section 3 briefly outlines an approa
h to timed rea
hability analysis of CANDLE models and introdu
es the main data stru
tures needed to support the analysis; sharing trees are introdu
ed in se
tion 4 and their appli
ation in rea
hability analysis is onsidered; related work is reviewed in section 5; section 6 concludes and proposes further work.

# 2 CANDLE

CANDLE is an expressive real-time language with a omparatively simple operational semanti
s. It has been developed for the modelling and analysis of realtime systems whi
h ommuni
ate using Controller Area Network (CAN) [9]. At the heart of  $CANDLE$ is a ore language, bCANDLE whi
h is a timed pro ess algebra allowing the expression of system models onsisting of a set of asyn
hronous pro
esses, ea
h having its own local data state and communicating by sending and re
eiving messages on one or more broadcast channels. A process can engage in three different kinds of basic action: 1) sending a message on a hannel; 2) re
eiving a message from a hannel and 3) performing an operation in a bounded amount of time, possibly transforming its lo
al data state on ompletion. More omplex pro
ess behaviour an be defined using sequential composition, guards on data states, non-deterministic choice and interrupt. A CANDLE system onsists of the asyn
hronous parallel composition of a fixed number of processes.

The semantics of a *CANDLE* system is given by asso
iating with it a timed transition system. A timed transition system  $S = (2, \sigma^-, L, \longrightarrow)$  is a tuple in which  $\Sigma$  is the set of states,  $\sigma^ \in$   $\Sigma$  is the initial state,  $L = A \cup \mathbb{R}^+$  is the set of labels consisting of *action* labels A and  $time$  labels  $\mathbb{R}^+$  and is required to be deterministi and ontinuous with respect to the passage of time. The semantics are given in detail in  $[10]$ . For the purposes of verifying a CANDLE system, we work with a timed safety automaton  $[8]$  having a bisimilar transition system. We introduce timed safety automata briefly below.

Let H be a set  $\{h_0, h_1, \dots, h_n\}$  of real-valued variables, called *clocks*, where each  $h_i \in H$  ranges over the non-negative reals  $\mathbb{R}$  . A *clock valuation* is a  $f$ unction  $\mathbf{v} : \mathbf{n} \to \mathbb{n}$  which assigns a value in  $\mathbb{n}$  to each clock in H. We assume that  $h_0$  is given the value  $\sigma$  by every clock valuation. We denote by  $\mathbf{v}|\mathbf{n}||:=\sigma|,$ the clock valuation  ${\bf v}$  such that  ${\bf v}$   $(n)$   $=$  0 for all  $h \in \Pi$  and  $\mathbf{v}(h) = \mathbf{v}(h)$  otherwise. For  $l \in \mathbb{R}^+,$ we denote by  $\mathbf{v} + \iota$  the clock valuation  $\mathbf{v}$  such that

 $\mathbf{v}(n) = \mathbf{v}(n) + t$  for all clocks in H. U is the clock valuation which assigns 0 to every clock. A bound over H is a constraint of the form  $h_i - h_j \# c$  where  $i, j \in \{0, \ldots, n\}, \# \in \{\lt, \leq\} \text{ and } c \in \mathbb{Z} \cup \infty.$  A clock constraint is a conjunction of bounds. We denote the set of clock constraints over the clocks H by  $\Phi(H)$ .

A timed safety automaton (TSA) is a tuple  $A =$  $(Q, q^-, A, E, \Pi, I)$  where: Q is a finite set of *control*  $u_0$ c $u_1$ ons,  $q^-$  is the initial control location,  $A$  is a finite set of event names,  $E$  is a finite set of edges where an edge is of the form  $(q, \varphi, a, \Lambda, q)$  where  $q, q \in \mathbb{Q}$  are control locations;  $\varphi \in \Psi(\Pi)$  is a clock constraint,  $a \in A$  is an event name and  $X \subseteq H$  is a set of clocks to be reset; H is a finite set of clocks, and  $I: Q \to \Phi(H)$  is a function which associates a time progress condition (or *invariant*) with each control location.

The semantics of the TSA  $A = (Q, q^-, A, E, H, I)$ is given by the times transformation system T [[ALL  $(2, \sigma^-, L, \longrightarrow)$  where  $\Delta$  is the set of pairs  $(q, v)$  such that  $q \in Q$  is a location of A and **v** is a clock valuation for H which satisfies the invariant  $I(q)$ ;  $\sigma^- = (q^-, \mathbf{0})$  is the initial state;  $\mathcal{L} = A \cup \mathbb{R}^+$  is the set of labels;  $\mathcal{L} = \mathcal{L}$  ,  $\mathcal{L} = \mathcal{L}$ relation ontaining transitions as follows:

- Time transitions: A state can change due to the elapse of time. There is a transition  $(q, \mathbf{v}) \rightarrow (q, \mathbf{v} + t)$  if for all  $t' \leq t$ ,  $\mathbf{v} + t'$  satisfies the invariant  $I(q)$ .
- Event transitions: A state can change by moving location. For each state  $(q, \mathbf{v}) \in \Sigma$ , if there is an edge  $(q, \varphi, a, \Lambda, q) \in E$  such that **v** satisfies  $\phi$ , then there is a transition  $(q, \mathbf{v}) \rightarrow (q', \mathbf{v} | X := 0).$

For a TSA derived from a CANDLE system model, a location comprises information about: 1) the urrently a
tive pro
ess terms, given as a set of integers  $\{p_1, p_2, \ldots, p_c\}$  for some variable number c where each  $p_i$  defines a marked place in a netlike representation of the process term for the model; 2) the values of all data variables, given as a sequen
e of values  $\langle v_1, v_2, \ldots, v_d \rangle$  for some fixed number d of variables; and 3) the state of the network hannels, given as a sequence of pairs  $(s, m)$  where s gives the status of the channel, *free*, *transmitting*, etc. and  $m$  is a variable-length, priority ordered sequence of messages awaiting transmission on the hannel. A CANDLE state vector, then, consists of a location as described above and a (set of) clock valuation(s), see figure 1.

# 3 Rea
hability Analysis

Of the several approa
hes to automated analysis of real-time systems, rea
hability analysis (RA) is one of the more easily implemented and informative. The basi rea
hability problem is to determine the set of system states which are encountered on any execution starting from some given state. RA allows the checking of *safety* properties of a system by answering the question: is it possible to reach an incorrect or unsafe state from an initial state. Other verifiation problems an be solved by building upon the solution of the basic RA problem  $[1]$ . Algorithm 1 outlines a basi algorithm for omputing the set of states rea
hable from a given initial state.

#### Algorithm 1 (Rea
hable States)

 $VISTED := \{(q^L, 0)\}\$  $WAITING := \{(q^L, 0)\}\$ while  $WAITING \neq \emptyset$  do remove some  $(q, D)$  from WAITING  $succ := \{ (q_s, D_s) : (q, D) \rightarrow (q_s, D_s) \land D_s \neq \emptyset \}$ for each  $(q_s, D_s) \in succ$  do  $\textbf{if } \forall (q_s, \mathrm{D}') \in \textit{VISITED} \bullet \mathrm{D}_s \nsubseteq \mathrm{D}'$ add  $(q_s, D_s)$  to VISITED add  $(q_s, D_s)$  to WAITING  $\mathbf f$ od od

The termination of the algorithm depends upon the construction of a finite quotient of the infinite transition system given by the TSA semantics. Important aspe
ts of su
h a onstru
tion are 1) the use of symbolic states  $(q, D)$  where q is a location as usual and D is a lo
k onstraint system whi
h represents the set of lo
k valuations satisfying it, and 2) the definition of a transition relation  $\rightarrow$  between symbolic states. Lack of space prevents us from giving further details here; the reader is referred to [15] for an ex
ellent dis
ussion of these issues.

The problem is to arrange for the compact storage of the set *VISITED* of visited state vectors, where a major difficulty has been to combine a good encoding of the locations (the discrete part of the system) with a good encoding for the clock valuations (the ontinuous part). This problem is addressed in the following se
tion.

### 4 Sharing trees

The sharing tree data structure [16] has been designed for the ompa
t storage of large sets of tuples. Their efficacy in the verification of untimed systems has been demonstrated; of particular interest to us is the work reported in  $[6, 7]$  which shows impressive spa
e redu
tions for sets of state ve
tors

$\{p_1, p_2, \ldots, p_c\}$		$\langle v_1, v_2, \dots, v_d \rangle$ $ \langle (s_1, m_1), (s_2, m_2), \dots, (s_n, m_n) \rangle$	$(\varphi_1, \varphi_2, \ldots, \varphi_r)$
Control	Data	Network	Clock Valuation
$\text{LOCATION}-q$			$CLOCK$ VALUATION(S) – D

Figure 1: Structure of a *bCANDLE* state vector

in which each vector is very similar to the location component of a CANDLE state vector.

**Definition 1**  $A$  sharing tree is a rooted acyclic  $graph(N, V, val, r, succ) where N = N_0 + N_1 \cdots +$  $N_k$ , with  $k \geq 0$ , is a finite set of nodes which are organised into  $k+1$  layers,  $N_i$  being the set of nodes of layer  $i, 0 \leq i \leq k$ ; V is a set of values,  $\top, \bot \notin V$ , with valuation function val :  $N \to V \cup \{\top, \bot\}$ ; r is the root node,  $N_0 = \{r\}$  and  $\forall n \in N$  • val $(n)$  =  $\cdots \iff n \in N_0; \; succ : N \to Z \; \; \; \text{is} \; \; \text{une} \; \; \text{such}$ cessor function which for a given node,  $n \in N_i$ , identifies the set of all nodes,  $succ(n) \subseteq N_{i+1}$ , which are directly descended from  $n$ ; and the following properties hold: 1)  $\forall i \mid 0 \leq i \leq k, \forall n \in$  $N \bullet succ(n) \subseteq N_{i+1}$ : each nodes has all of its successors in the next layer; 2)  $\forall n \in N, \forall s_1, s_2 \in$  $succ(N) \bullet s_1 \neq s_2 \implies val(s_1) \neq val(s_2)$ : a node does not have distinct successors with equal values; 3)  $\forall i \mid 0 \leq i \leq k, \forall n_1, n_2 \in N_i \mid n_1 \neq n_2$  $val(n_1) = val(n_2) \implies succ(n_1) \neq succ(n_2):$  if 2 or more nodes in the same layer have the same values then they have different sets of successors;  $\{A\}$   $\forall n \in N \bullet val(n) = \bot \implies succ(n) = \emptyset \; \mathit{5}$   $\forall n \in N$  $N \bullet succ(n) = \emptyset \implies (val(n) = \bot \vee val(n) = \top)$ 

The elements of a sharing tree are just those tuples of values which occur by following a path from the root node to a node whose value is  $\perp$ . For example, figure 2 shows a sharing tree representing the set of tuples:  $\{(a, b, d), (a, c, d), (a, b, d, e, g), (a, b, d, f, g),\}$  $(a, c, d, e, g), (a, c, d, f, g)$ 

The data compression achieved by a sharing tree arises from the guaranteed sharing of all identi
al prefixes and a 'best-effort' sharing of identical suffixes. It is clear that a set of state vectors will usually contain many states that differ in few components and so allow for onsiderable sharing. The use of a sharing tree for the state store in a rea
hability analysis requires the partitioning of ea
h state vector (figure 1) into a tuple of values, where each tuple omponent is allo
ated to a distin
t layer in the tree. The mapping of components of the state vector into tuple components and the ordering of components within tuples can have a significant impact upon the space reductions achieved [7]. An important property of a sharing tree is that it can contain tuples of differing lengths. This allows considerable discretion in the mapping of variable length components of the state ve
tor, for example the message



Figure 2: Sharing Tree Example

queues. The key observation on
erning the suitability of sharing trees in the analysis of timed systems is that the lo
k onstraint omponent D of a symbolic state  $(q, D)$  can be represented simply by one or more omponents of the omplete state tuple and so an be easily in
orporated into the state store. This contrasts significantly with approaches based upon a BDD representation of the state store where this integration is mu
h more problemati
.

# 5 Related work

Representation of timing onstraints by DBMs was proposed by Dill [5] and has been preferred in the most efficient verification tools for timed systems, such as KRONOS [8] and UPPAAL [12].

Wong-Toi and Dill [14] and Balarin [3] have each shown techniques for encoding DBMs using BDDs and incorporating them into BDD encodings of the transition relation, approximating unions of zones using convex hulls. Bozga et. al. [4] offer a canonical representation of discretized sets of clock config $urationality$  is  $|2|$ , which are a BDD-based encoding amenable to combination with a symbolic representation of the discrete part of the system.

Larsen et. al. [11] propose a compact encoding

<sup>1</sup>Numeri
al De
ision Diagrams

for DBMs which provides a minimal and canonical representation of clock constraints and allows for efficient inclusion checking between constraint systems. They do not consider how this representation may be combined with a symbolic representation of the rest of the system. Their approa
h is orthogonal to ours and it would be interesting to consider their combination experimentally.

Larsen et. al.  $[13]$  have recently proposed clock difference diagrams as a data structure for the compa
t representation of unions of zones. CDDs show some similarities both with BDDs and sharing trees. As far as we know, they remain to be used in practice

#### Conclusions and further work 6

In this paper, we have proposed the use of sharing trees for the representation of the state spa
e in the rea
hability analysis of timed systems. We believe that there is good reason to suppose that such a representation will offer significant space reduction, particularly in the analysis of asynchronous, data-bearing systems. The use of this representation omes with a time ost by omparison with the use of a traditional hash table but there is no reason to suppose that this penalty will be any greater in the analysis of timed systems than it is in the analysis of untimed systems where it has been shown to be acceptable in many circumstances [6, 7]. These conclusions remain to be confirmed by experiment.

# Referen
es

- [1] L. Aceto, A. Burgueño, and K. Larsen. Model he
king via rea
hability testing for timed automata. Technical report, BRICS, Aarhus University, 1997.
- [2] E. Asarin, M. Bozga, A. Kerbrat, O. Maler, A. Pnueli, and A. Rasse. Data stru
tures for the verification of timed automata. In O. Maler, editor, Pro
. 1st Int. Workshop on Hybrid and Real-Time Systems (HART'97), volume 1201 of Lecture Notes in Computer Science, pages 346– 360. Springer Verlag, Mar
h 1997.
- [3] F. Balarin. Approximate reachability analysis of timed automata. In Pro
. of 17th IEEE Real Time Systems Symposium, pages  $52{-}61$ . IEEE Computer Society Press, 1996.
- [4] M. Bozga, O. Maler, A. Pnueli, and S. Yovine. Some progress in the symbolic verification of timed automata. volume 1254 of Lecture Notes in Computer Science, pages  $179-190$ , Haifa, Israel, June 1997. Springer Verlag.
- [5] D. Dill. Timing assumptions and verification of finite state concurrent systems. In J. Sifakis,

editor, Automatic Verification Methods for Finite State Systems, volume 407 of Le
ture Notes in Computer Science, pages 197-212. Springer Verlag, 1989.

- [6] F. Gagnon, J.-C. Grégoire, and D. Zampunieris. Sharing tree for "on-the-fly" verification. In Proc. Int. Conf. on Formal Description Techniques VIII (FORTE'95). IEEE Computer So ciety Press, 1995.
- [7] J.-Ch. Grégoire. State space compression in SPIN with ge-sets. In Proc. 2nd SPIN Workshop, Rutgers University, New Jersey, USA, August 1996.
- [8] T. Henzinger, X. Nicollin, J. Sifakis, and S. Yovine. Symbolic model checking for realtime systems. Information and Computation,  $111(2):193-244, 1994.$
- [9] ISO/DIS 11898: Road Vehicles  $=$  interchange of digital information  ${\bf -$  Controller Area Network (CAN) for high speed ommuni
ation, 1992.
- [10] D. Kendall, S. Bradley, W.D. Henderson, and A.P. Robson. bCANDLE: Formal modelling and analysis of CAN control systems. In Proceedings of 4th IEEE Real Time Te
hnology and Appli cations Symposium  $(RTAS'98)$ , pages 171–177. IEEE Computer So
iety Press, June 1998.
- [11] K. Larsen, F. Larsson, P. Pettersson, and Wang Yi. Efficient verification of real-time systems: Compact data structure and state-space reduction. In Proc. of 18th IEEE Real Time Systems Symposium, De
ember 1997.
- [12] K. Larsen, P. Pettersson, and Wang Yi. UPPAAL in a Nutshell. Springer International Journal on Software Tools for Te
hnology Transfer, O
tober 1997.
- [13] K. Larsen, C. Weise, Wang Yi, and J. Pearson. Clock difference diagrams. Technical Report Nr 98/99, DoCs, Uppsala University, August 1998. ISSN 0283-0574.
- [14] H. Wong-Toi and D. Dill. Approximations for verifying timing properties. In T. Rus and C. Rattray, editors, Theories and Experien
es for Real-time System Development. World Scientific Publishing, 1994.
- [15] S. Yovine. Model checking timed automata. In G. Rozenberg and F. Vaandrager, editors, Embedded Systems, Papers from the European Edu
ational Forum S
hool on Embedded Systems, Veldhoven. The Netherlands, Lecture Notes in Computer S
ien
e. Springer Verlag, 1997.
- [16] D. Zampuniéris. The Sharing Tree Data Structure. PhD thesis, Facultés Universitaires Notre-Dame de la Paix, Namur, Belgium, May 1997.